

Claims

What we claim is:

5 [0032] 1. A method for actively adjusting the back bias voltage of one or more CMOS transistors comprising the steps:
fabricating a reference transistor on a chip,
monitoring the leakage current of the reference transistor with
an active dc output control circuit, and
10 adjusting the back bias voltage of the well containing the
reference transistor until the leakage current is below a
preset value.

[0033] 2. The method of claim 1 wherein said reference transistor
15 comprises a P-MOS transistor in a P-MOS well or a N-MOS
transistor in a N-MOS well.

[0034] 3. The method of claim 1 wherein said monitoring and said
adjusting are performed by an active dc output control circuit
20 not on the same chip as the reference transistor.

[0035] 4. The method of claim 1 wherein said active dc output control
circuit monitors and adjusts at least one P-MOS well and at

least one N-MOS well.

[0036] 5. The method of claim 1 wherein there is one or more active dc
output control circuits on the same chip with one or more said
5 reference transistors.

[0037] 6. The method of claim 1 wherein said preset leakage value is
determined by the mask design of said active dc output control
circuit.

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[0038] 7. The method of claim 1 wherein said preset leakage value is
stored in programmable circuit elements of said active
dc output control circuit after fabrication.

15 [0039] 8. The method of claim 7 wherein said preset leakage value is
stored in re-programmable circuit elements of said active
dc output control circuit after fabrication.

[0040] 9. The method of claim 8 wherein said active dc output control
20 circuit processes a signal to set said preset leakage value in
said reprogrammable circuit elements of said active
dc output control circuit.

[0041] 10. The method of claim 9 wherein said active dc output control circuit contains re-programmable circuit elements and addressing means for one or more preset leakage values.

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[0042] 11. An integrated circuit for actively adjusting the back bias voltage of one or more CMOS transistors comprising:
a means for monitoring the leakage current of a reference transistor on a chip,
10 a means for adjusting the back bias voltage of the well containing the reference transistor,
a means for determining when the leakage current is below a preset value, and
a means for maintaining the back bias voltage and the leakage
15 current in a narrow range.

[0043] 12. The integrated circuit of claim 11 wherein said integrated circuit is not on the same chip as the reference transistor.

20 [0044] 13. The integrated circuit of claim 11 wherein said reference transistor comprises a P-MOS transistor in a P-MOS well or a N-MOS transistor in a N-MOS well.

[0045] 14. The integrated circuit of claim 11 wherein said leakage current
preset values are stored in programmable memory.

[0046] 15. The integrated circuit of claim 11 further comprising a means
5 to adjust the back bias of a well not containing the
reference transistor.

[0047] 16. An integrated circuit for actively adjusting one or more of its
output voltages based on monitoring the current of one
10 or more CMOS transistors comprising:
a means for monitoring the current of one or more
CMOS transistors,
a means for adjusting one or more of its output
voltages,
15 a means for determining when the monitored one or
more currents is below a preset value,
a means for maintaining its one or more output voltages
in a narrow range, and
a means for storing the preset values in
20 programmable memory.

[0048] 17. An integrated circuit for actively adjusting the threshold voltage

of one or more CMOS transistors comprising:

a means for monitoring the leakage current of a reference

transistor on a chip;

5 a means for adjusting the back bias voltage of the well

containing the reference transistor;

a means for determining when the leakage current is about a

preset value;

a means for maintaining the back bias voltage and the leakage

10 current in a narrow range; and

a means for correlating said leakage current with the threshold

voltage.